EMIF03-SIM01

3 LINES EMI FILTER AND ESD PROTECTION

IPAD™

MAIN PRODUCT APPLICATIONS

EMI filtering and ESD protection for :

- SIM Interface (Subscriber Identify Module)
- UIM Interface (Universal Identify Module)

DESCRIPTION

The EMIF03-SIM01 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF03 Flip Chip packaging means the package size is equal to the die size.
This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

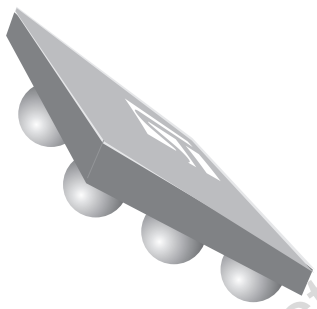
BENEFITS

- EMI symmetrical (I/O) low-pass-filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.57mm x 1.57 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS :

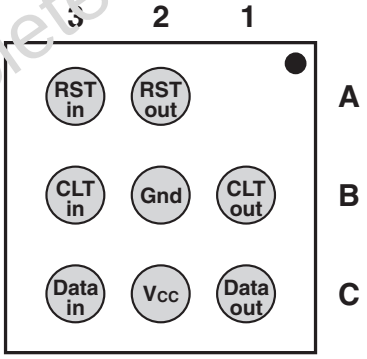
IEC61000-4-2 15kV (air discharge)
8 kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3

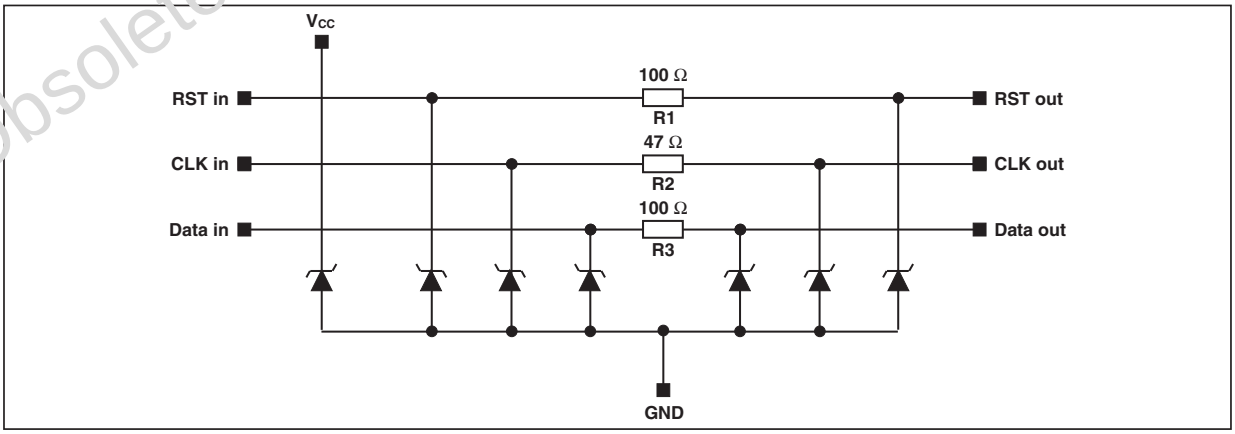


Flip Chip package

PIN CONFIGURATION (Ball side)



CONFIGURATION



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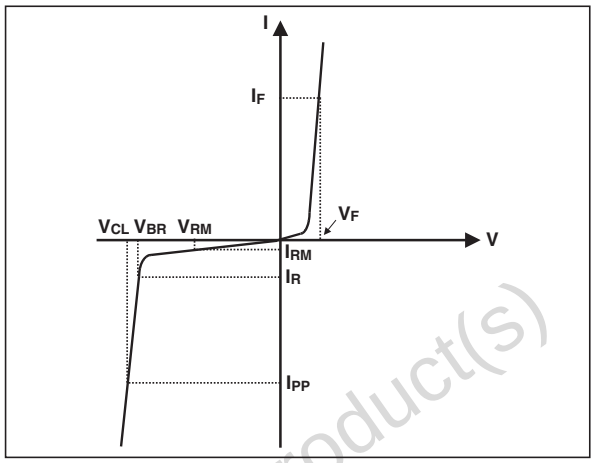
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
Rd	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
Cline	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3V			1	µA
R_d			1.5		Ω
R_1		95	100	105	Ω
R_2		44.65	47	49.35	Ω
R_3		95	100	105	Ω
C_{line}	@ 0V			35	pF

Fig. 1: S21 (dB) attenuation measurements.

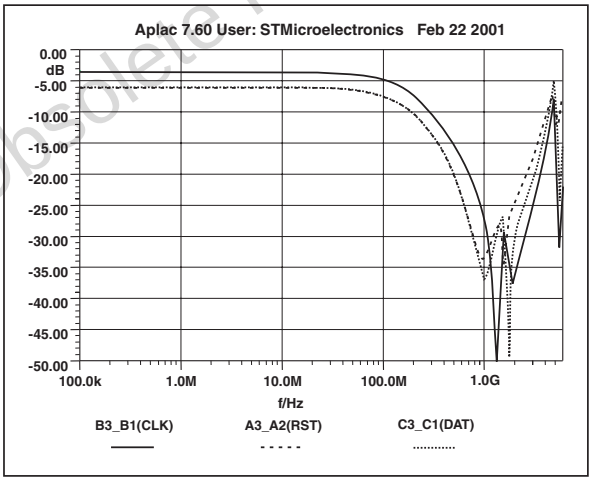


Fig. 2: Analog crosstalk measurements.

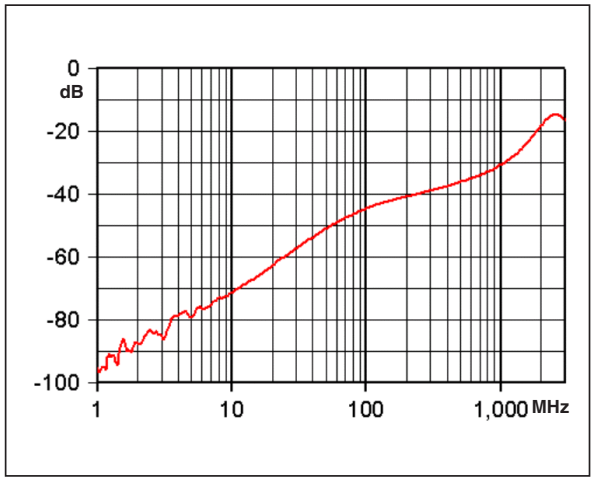


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Fig. 3: Digital crosstalk measurements.

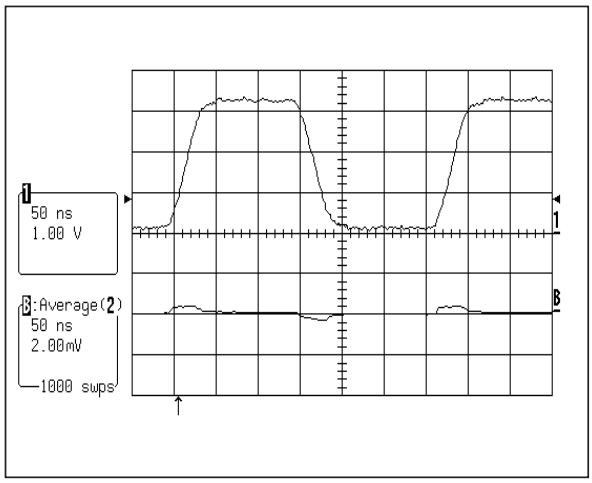


Fig. 4: ESD response to IEC61000-4-2 (+15kV air discharge) on one input and on one output.

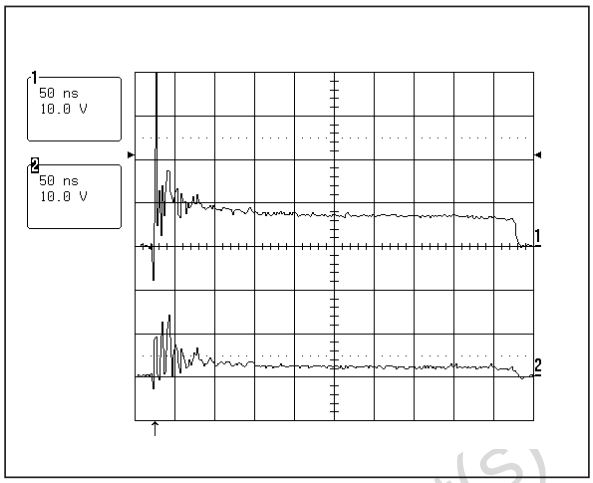


Fig. 5: ESD response to IEC61000-4-2 (-15kV air discharge) on one input and on one output.

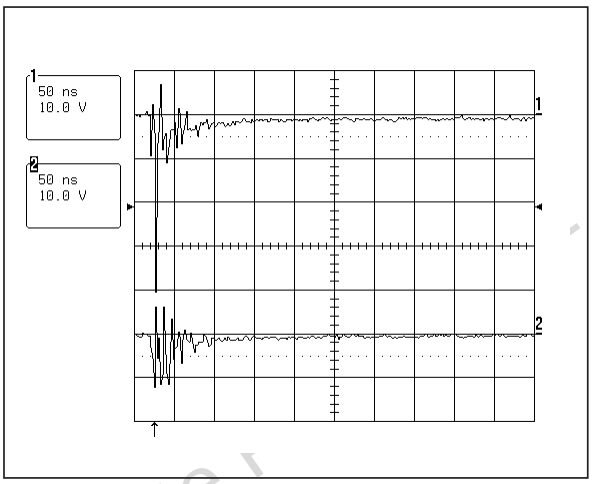
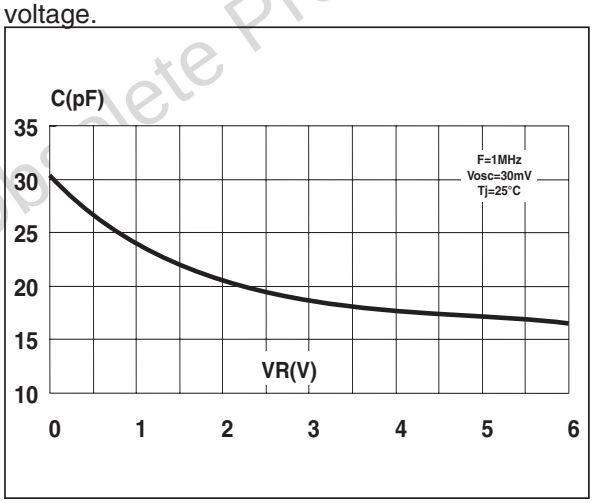


Fig. 6: Line capacitance versus reverse applied voltage.



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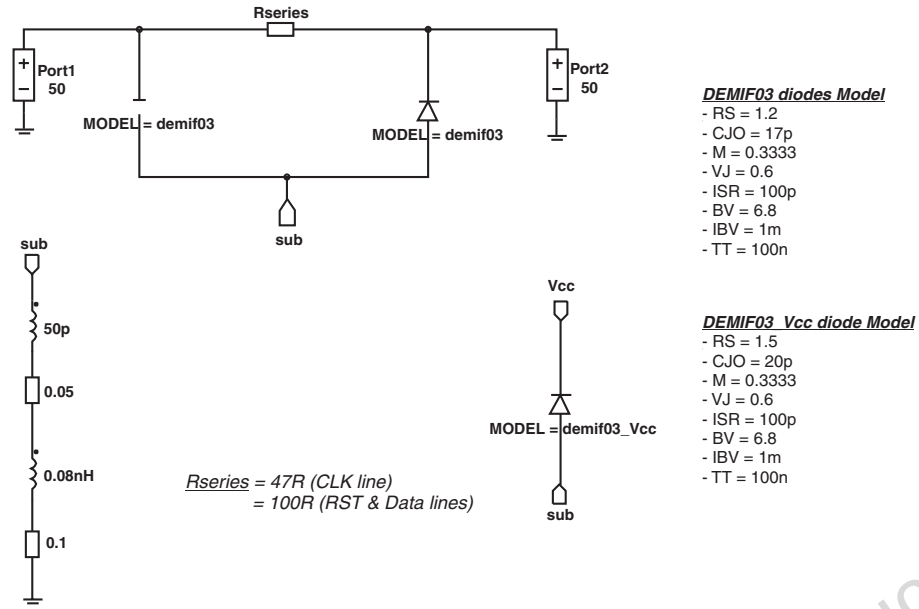
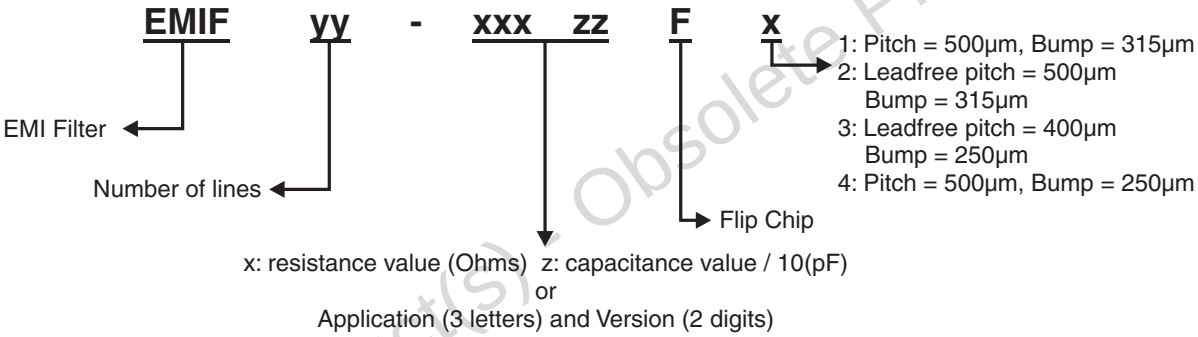
Aplac model

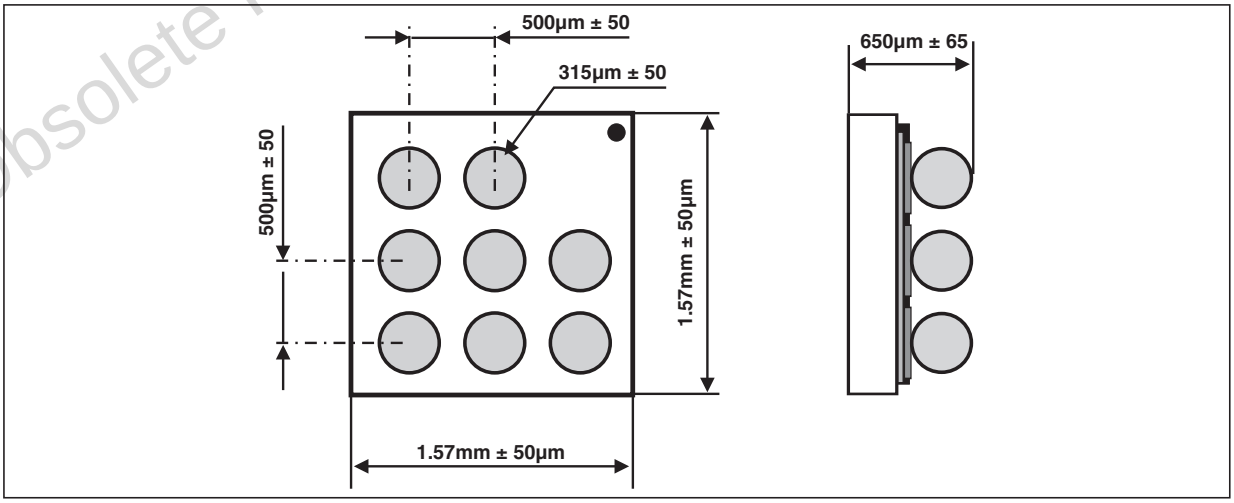


ORDER CODE



PACKAGE MECHANICAL DATA

(all dimensions in µm)



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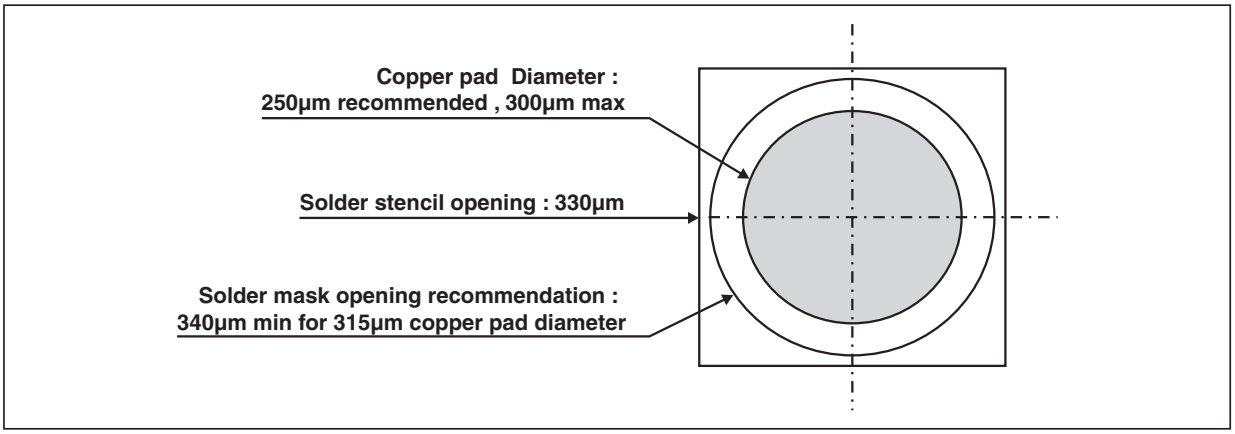
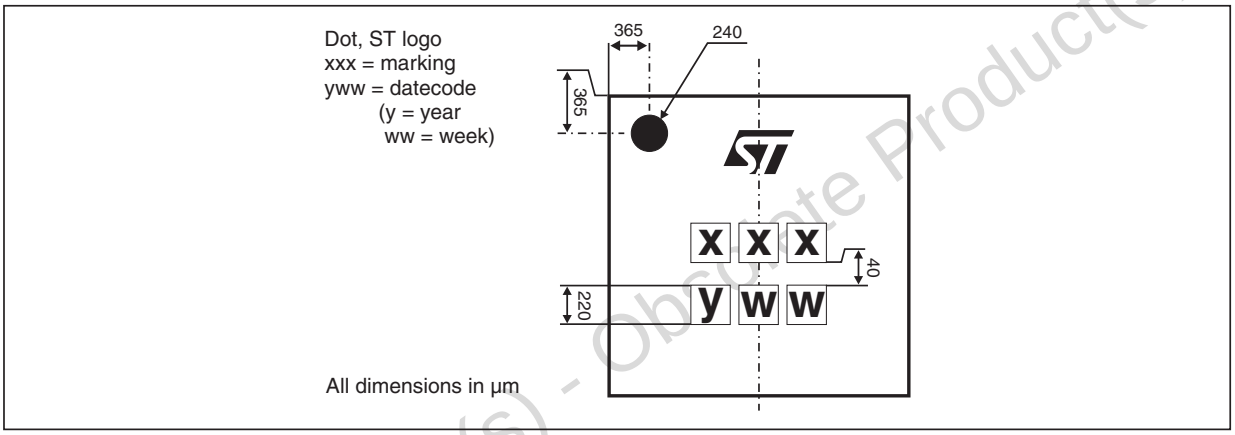
FOOT PRINT RECOMMENDATIONS



MARKING



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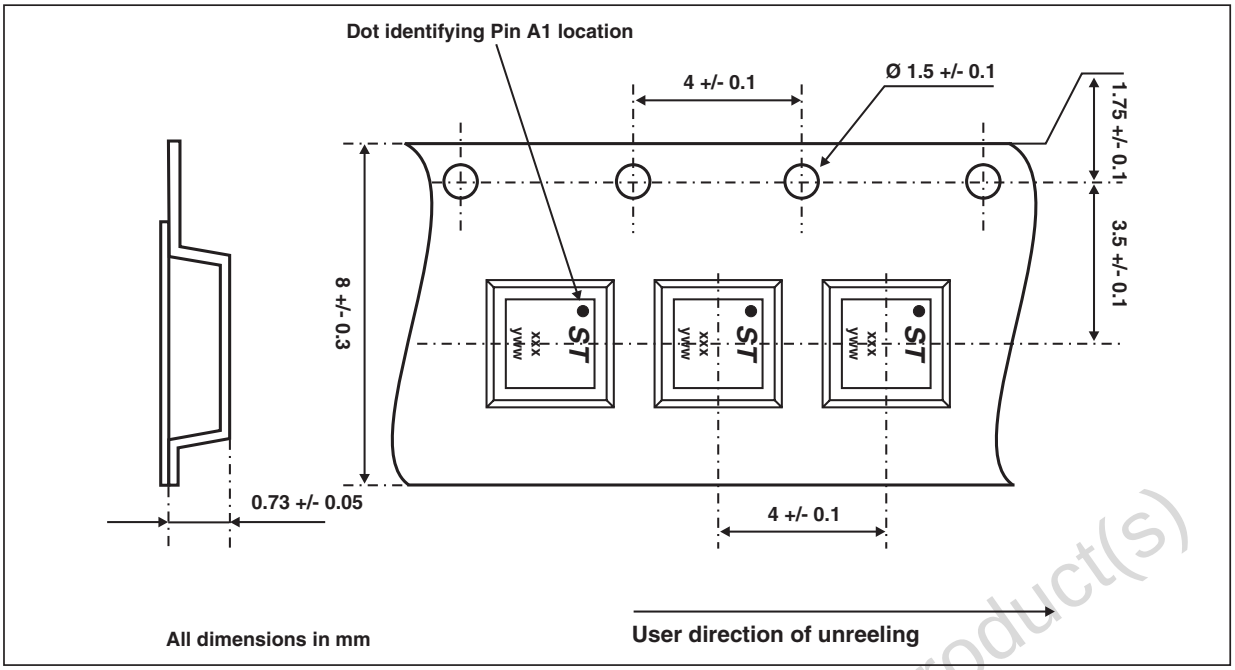
PACKING



PACKING

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM01	FCT	Flip Chip	3.3 mg	5000	Tape & reel 7”

Note: More packing information are available in the application note AN1235: “Flip-Chip: Package description and recommendations for use”

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