

# FDZ293P

## P-Channel 2.5 V Specified PowerTrench® BGA MOSFET

### General Description

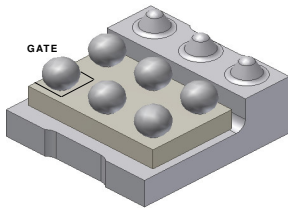
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ293P minimizes both PCB space and  $r_{DS(on)}$ . This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low  $r_{DS(on)}$ .

### Applications

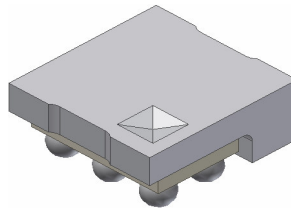
- Battery management
- Load switch
- Battery protection

### Features

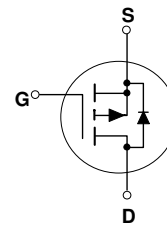
- -4.6 A, -20 V  $r_{DS(on)} = 46 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$   
 $r_{DS(on)} = 72 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Occupies only 2.25 mm<sup>2</sup> of PCB area.  
Less than 50% of the area of a SSOT-6
- Ultra-thin package: less than 0.85 mm height when mounted to PCB
- Outstanding thermal transfer characteristics:  
4 times better than SSOT-6
- Ultra-low  $Q_g \times r_{DS(on)}$  figure-of-merit
- High power and current handling capability.



Bottom



Top



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DS</sub>	Drain-Source Voltage	-20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	-4.6	A
		-10	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a)	1.7	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	72	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	2	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
B	FDZ293P	13"	8mm	10000 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-13		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-0.8	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -4.6\text{ A}$ , $V_{GS} = -2.5\text{ V}, I_D = -3.6\text{ A}$ , $V_{GS} = -4.5\text{ V}, I_D = -4.6\text{ A}, T_J = 125^\circ\text{C}$		36 58 47	46 72 65	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-10			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -4.6\text{ A}$		13		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		754		pF
$C_{oss}$	Output Capacitance			167		pF
$C_{rss}$	Reverse Transfer Capacitance			92		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		6		$\Omega$

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A}, V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		11	20	ns
$t_r$	Turn-On Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
$t_f$	Turn-Off Fall Time			17	31	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -4.6\text{ A}, V_{GS} = -4.5\text{ V}$		7.5	11	nC
$Q_{gs}$	Gate-Source Charge			1.5		nC
$Q_{gd}$	Gate-Drain Charge			2.0		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

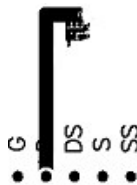
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.4	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.4\text{ A}$ (Note 2)		-0.7	-1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = -4.6\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		17		nS
$Q_{rr}$	Diode Reverse Recovery Charge			5		nC

**Notes:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball,  $R_{\theta JB}$ , is defined for reference. For  $R_{\theta JC}$ , the thermal reference point for the case is defined as the top surface of the copper chip carrier.  $R_{\theta JC}$  and  $R_{\theta JB}$  are guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



- 72°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB



- 157°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

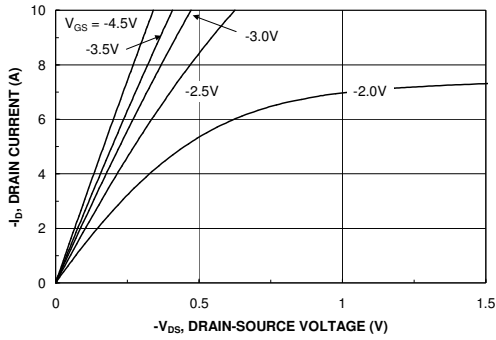


Figure 1. On-Region Characteristics.

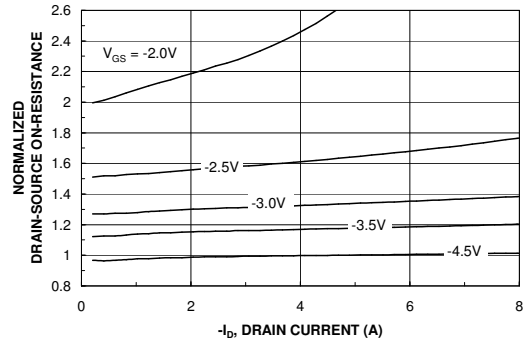


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

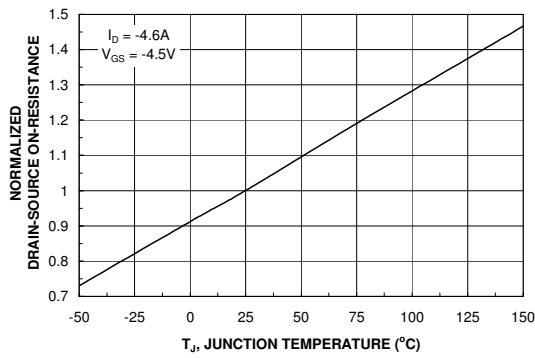


Figure 3. On-Resistance Variation with Temperature.

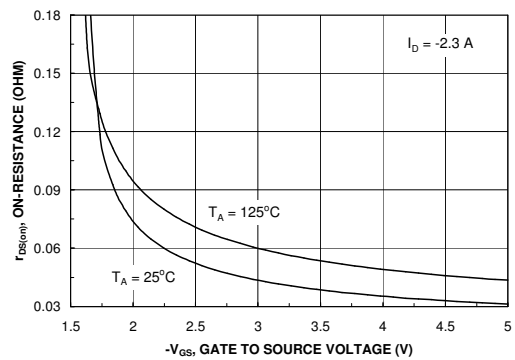


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

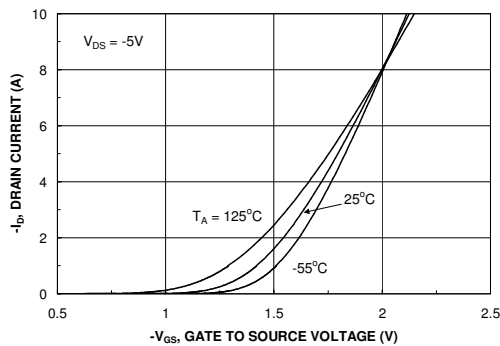


Figure 5. Transfer Characteristics.

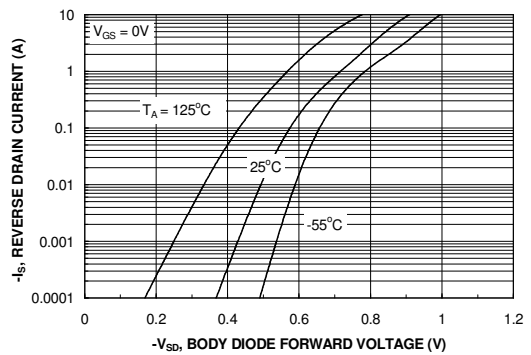


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

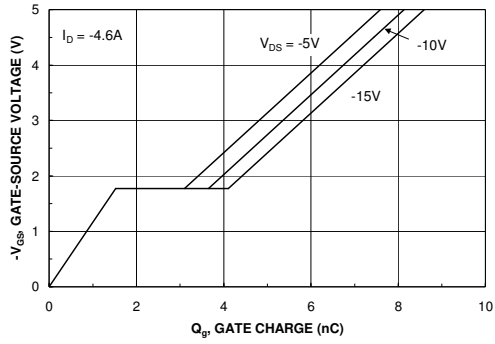


Figure 7. Gate Charge Characteristics.

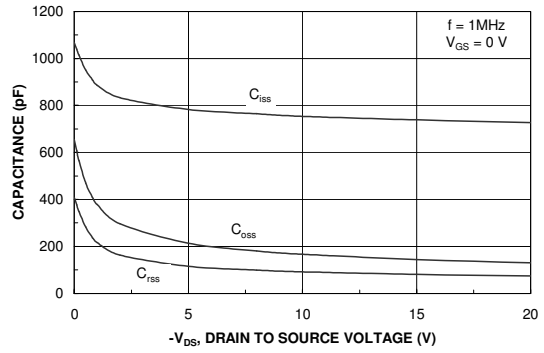


Figure 8. Capacitance Characteristics.

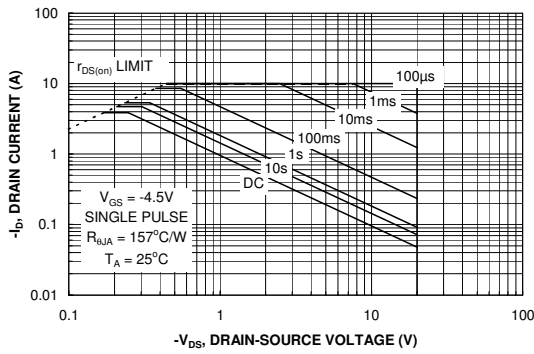


Figure 9. Maximum Safe Operating Area.

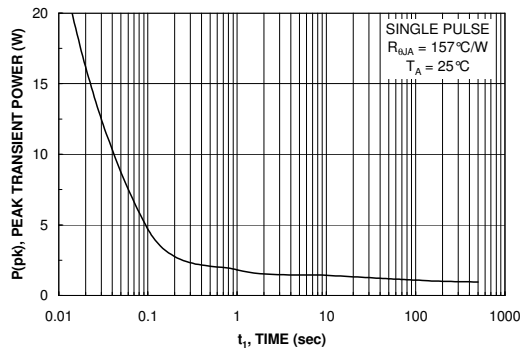


Figure 10. Single Pulse Maximum Power Dissipation.

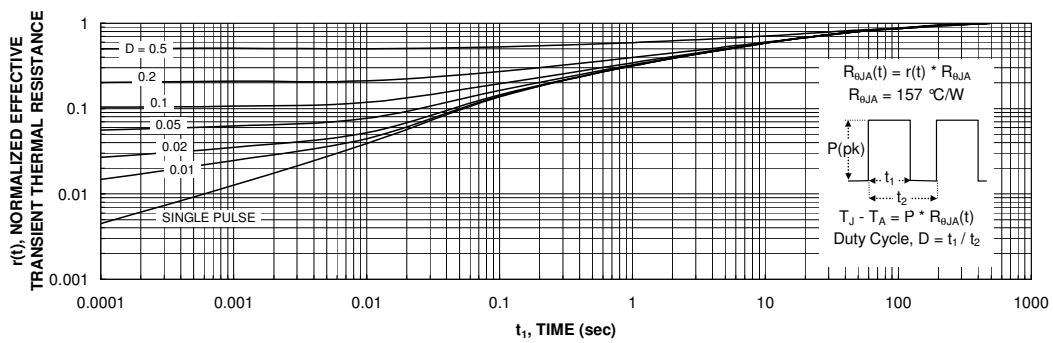
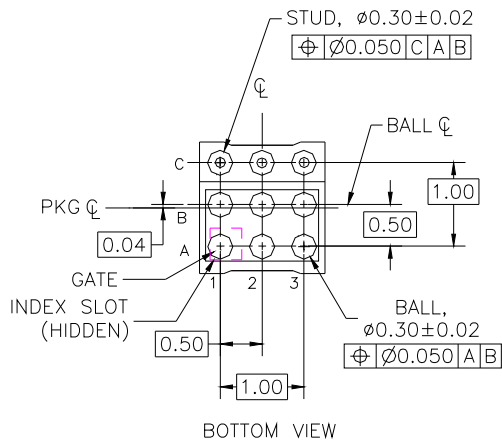
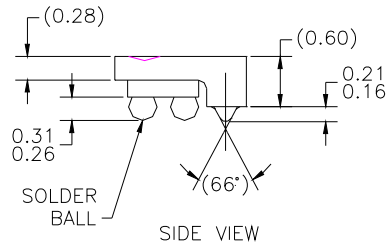
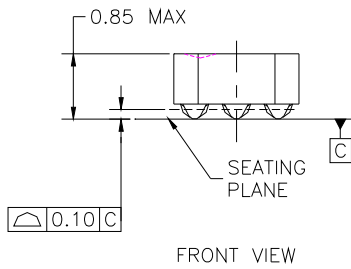
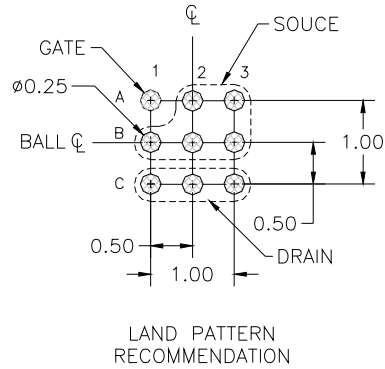
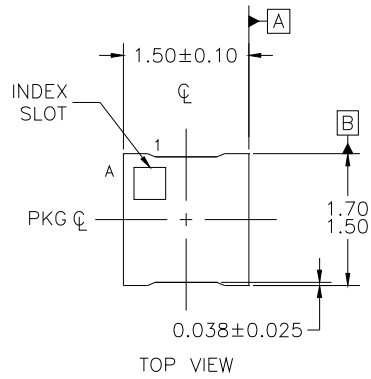


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

## Dimensional Pad and Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF SEPTEMBER 2003.
- C) BALL/STUD CONFIGURATION TABLE

TERMINAL ID	DESIGNATION	TERMINAL TYPE
C1,C2,C3	DRAIN	COPPER STUD
A1	GATE	BALL
A2,A3,B1,B2,B3	SOURCE	BALL

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