

## 74ACT823 9-Bit D-Type Flip-Flop

### General Description

The ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACT823 offers noninverting outputs.

### Features

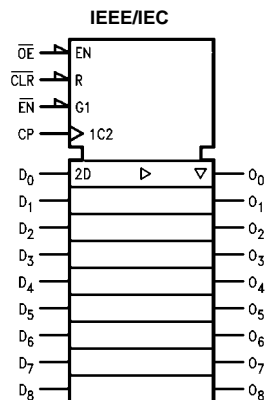
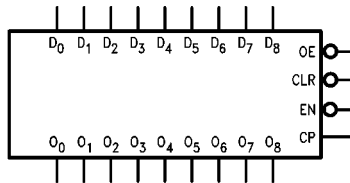
- Outputs source/sink 24 mA
- 3-STATE outputs for bus interfacing
- Inputs and outputs are on opposite sides
- TTL compatible inputs

### Ordering Code:

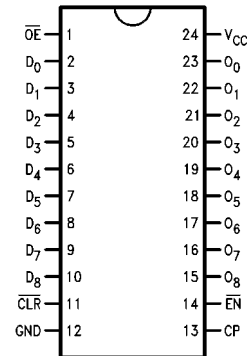
Order Number	Package Number	Package Description
74ACT823SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT823MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT823SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (SPC not available in Tape and Reel.)

### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>8</sub>	Data Inputs
O <sub>0</sub> -O <sub>8</sub>	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

FACT™ is a trademark of Fairchild Semiconductor Corporation.

## Functional Description

The ACT823 consists of nine D-type edge-triggered flip-flops. These have 3-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{OE}$  LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. In addition to the Clock and Out-

put Enable pins, there are Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins. These devices are ideal for parity bus interfacing in high performance systems.

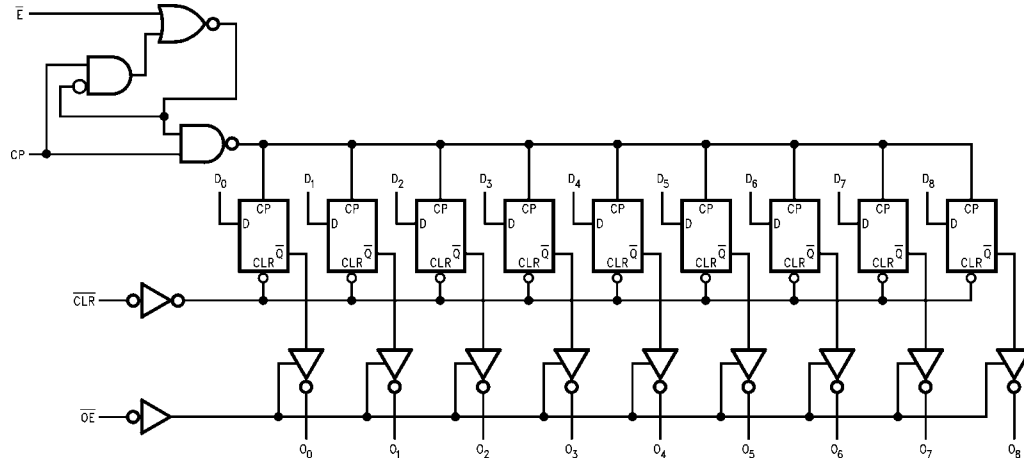
When  $\overline{CLR}$  is LOW and  $\overline{OE}$  is LOW, the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{EN}$  is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

## Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↗	L	L	Z	High Z
H	X	L	↗	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to 7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
$V_{IL}$	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.5	0.8	0.8			
$V_{OH}$	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
			5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$	
				4.86	4.76			
$V_{OL}$	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$	
		5.5		0.36	0.44			
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OZ}$	Maximum 3-STATE Current	5.5		$\pm 0.5$	$\pm 5.0$	$\mu A$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$	
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
$I_{CC}$	Maximum Quiescent Supply Current	5.5		8.0	80	$\mu A$	$V_{IN} = V_{CC}$ or GND	

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 4)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	5.0	120	158		109		MHz
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.5	5.5	9.5	1.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	2.0	5.5	9.5	1.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	5.0	2.5	8.0	13.5	2.0	15.5	ns
t <sub>PZH</sub>	Output Enable Time OE to O <sub>n</sub>	5.0	1.5	6.0	10.5	1.5	11.5	ns
t <sub>PZL</sub>	Output Enable Time OE to O <sub>n</sub>	5.0	2.0	6.5	11.0	1.5	12.0	ns
t <sub>PHZ</sub>	Output Disable Time OE to O <sub>n</sub>	5.0	1.5	6.5	11.0	1.5	12.0	ns
t <sub>PLZ</sub>	Output Disable Time OE to O <sub>n</sub>	5.0	1.5	6.0	10.5	1.5	11.5	ns

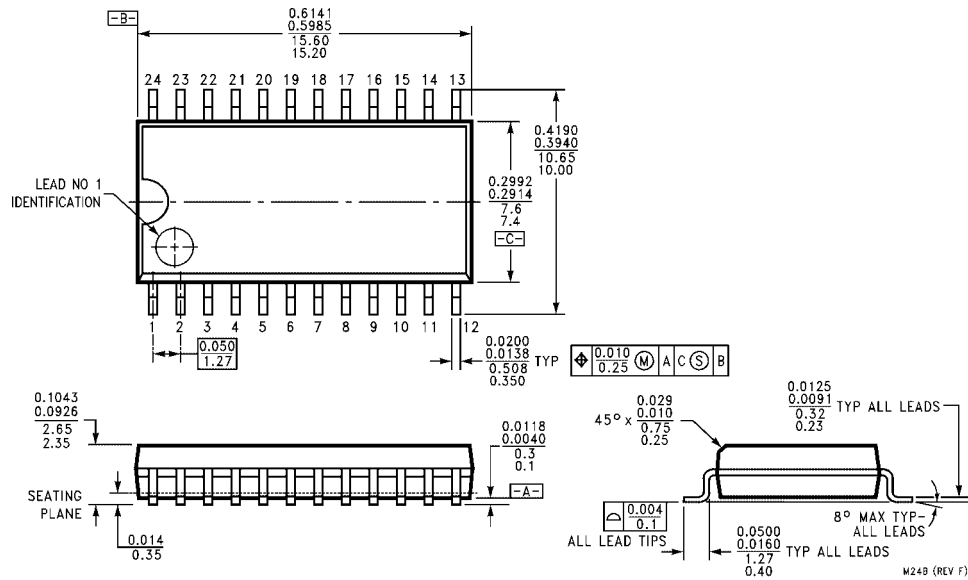
Note 4: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C	Units
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW D to CP	5.0	0.5	2.5	2.5	ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0	2.5	2.5	ns
t <sub>S</sub>	Setup Time, HIGH or LOW EN to CP	5.0	0	2.0	2.5	ns
t <sub>H</sub>	Hold Time, HIGH or LOW EN to CP	5.0	0	1.0	1.0	ns
t <sub>W</sub>	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	5.5	ns
t <sub>W</sub>	CLR Pulse Width, LOW	5.0	3.0	5.5	5.5	ns
t <sub>REC</sub>	CLR to CP Recovery Time	5.0	1.5	3.5	4.0	ns

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V

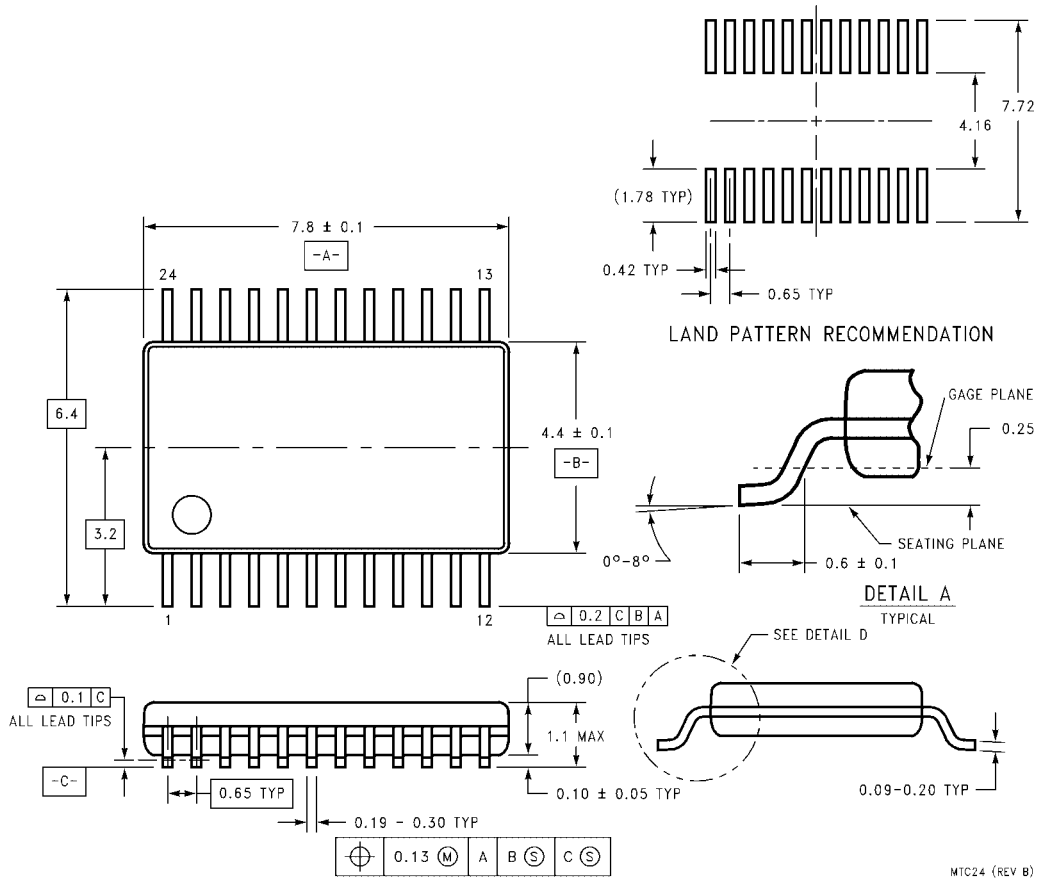
Capacitance				
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	44	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



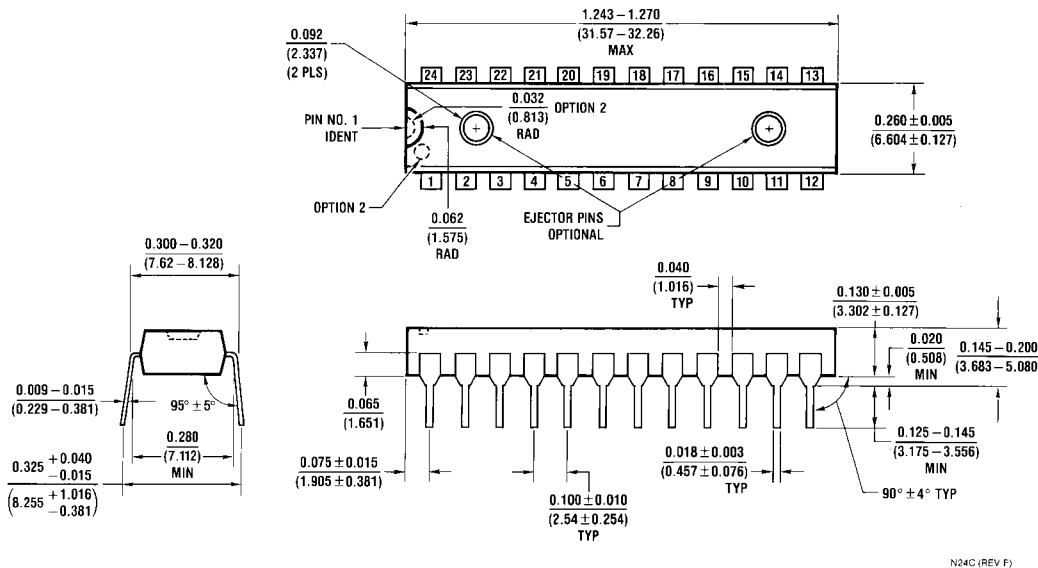
**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)